CLAIMS

We claim:

1. A switching regulator for receiving an input voltage and generating an output voltage having substantially constant magnitude, the switching regulator comprising:

an error amplifier having a first input node coupled to receive a first voltage corresponding to the output voltage, a second input node coupled to a reference voltage and an output node providing an error voltage indicative of the difference between the first voltage and the reference voltage;

a control circuit comprising an input node receiving the error voltage and an output node generating a first switch control signal and a second switch control signal, the first and second switch control signals driving a first switch and a second switch respectively for generating a signal for generating the output voltage, wherein the error amplifier and the control circuit form a feedback control loop having a first loop gain for maintaining the output voltage at a substantially constant magnitude; and

a compensation circuit disposed in the feedback control loop, the compensation circuit applying a scaling factor to the first loop gain,

wherein the first loop gain of the feedback control loop is defined by a first function describing a the loop gain dependency on the input voltage and the output voltage, and the compensation circuit applies a second function describing the scaling factor wherein the second function is a reciprocal function of the first function.

2. The switching regulator of Claim 1, wherein the error amplifier comprises an output circuit and the compensation circuit is coupled in series with the output circuit of the error amplifier.

3. The switching regulator of Claim 1, wherein the compensation circuit is coupled to circuitry within the error amplifier.

4. The switching regulator of Claim 1, wherein the first loop gain is defined by a first function being the ratio of the input voltage to the output voltage, and the second function is indicative of a ratio of the output voltage to the input voltage.

5. The switching regulator of Claim 4, wherein the control circuit comprises a PWM comparator receiving the error voltage and a ramp voltage as input signal and generating a PWM output voltage, and a driver circuit coupled to receive the PWM output voltage and generating the first and second switch control signals, and wherein the scaling factor described by the second function comprises the average of the PWM output voltage.

6. The switching regulator of Claim 4, wherein the first switch and the second switch are coupled to drive a switch output node, the first switch being turned on to decrease the current provided to the switch output node and the second switch being turned on to increase the current provided to the switch output node.

7. The switching regulator of Claim 6, wherein the scaling factor described by the second function comprises the duty cycle of the switching regulator.

8. The switching regulator of Claim 6, wherein the scaling factor described by the second function comprises an average of second switch control signal driving the second switch.

9. The switching regulator of Claim 6, wherein the switching regulator comprises a voltage mode buck regulator and the first loop gain is given as $V_{Ref}A_{VEA}V_{IN}/V_{OUT}$, where V_{Ref} is the reference voltage, A_{VEA} is the gain of the error amplifier, V_{IN} is the input voltage, and V_{OUT} is the output voltage, and wherein the second function is given as $(1 + t_{ON,M2}/t_{ON,M1})$ which is equivalent to V_{OUT}/V_{IN}, where $t_{ON,M2}$ represents the on-time of the second switch and $t_{ON,M1}$ represents the on-time of the first switch.

10. The switching regulator of Claim 9, wherein the switching regulator is being operated in a continuous conduction mode and the second function is given as $(t_{ON,M2}/T_{cycle})$ which is equivalent to V_{OUT}/V_{IN}, wherein T_{cycle} is the system clock cycle time of the switching regulator.

11. The switching regulator of Claim 9, wherein the compensation circuit comprises:

a first low pass filter for filtering the first switch control signal;

a second low pass filter for filtering the second switch control signal;

a first divider circuit coupled to receive the filtered first switch control signal and the filtered second switch control signal and generate a first divider output signal indicative of the ratio of the filtered first switch control signal to the filtered second switch control signal;

a summing circuit coupled to sum the first divider output signal with a second voltage and generating a summed output voltage; and

a second divider circuit coupled to receive the summed output voltage and the second voltage and generate a second divider output signal indicative of the ratio of the summed output voltage to the second voltage,

wherein the second divider output signal has a value of $(1 + t_{ON,M2}/t_{ON,M1})$.

12. The switching regulator of Claim 11, wherein the second voltage comprises a power supply voltage of the error amplifier and the control circuit.

13. A method for providing compensation in a switching regulator receiving an input voltage and generating an output voltage having substantially constant magnitude, comprising:

determining a loop gain of a feedback control loop in the switching regulator;

determining a first function describing the loop gain dependency on the input voltage and the output voltage;

determining a second function being a reciprocal of the first function; and

applying the second function to a point in the feedback control loop of the switching regulator.

14. The method of Claim 13, wherein applying the second function to a point in the feedback control loop of the switching regulator comprises applying a scaling factor described by the second function to scale the loop gain of the feedback control loop.

15. The method of Claim 13, wherein applying the second function to a point in the feedback control loop of the switching regulator eliminates the loop gain dependency on the input voltage and the output voltage.

16. The method of Claim 13, wherein the switching regulator comprises an error amplifier in the feedback control loop, the error amplifier being coupled to compare a voltage indicative of the output voltage and a reference voltage and generate an error output voltage, and wherein applying the second function to a point in the feedback control loop of the switching regulator comprises providing a circuit implementing the second function and coupling the circuit implementing the second function in series an output circuit of the error amplifier.

17. The method of Claim 13, wherein the switching regulator comprises an error amplifier in the feedback control loop, the error amplifier coupled to compare a voltage indicative of the output voltage to a reference voltage and generate an error output voltage, and wherein applying the second function to a point in the feedback control loop of the switching regulator comprises providing a circuit implementing the second function and coupling the circuit implementing the second function to circuitry within the error amplifier.

18. The method of Claim 13, wherein the first function is defined by the ratio of the input voltage to the output voltage, and the second function is indicative of a ratio of the output voltage to the input voltage.

19. The method of Claim 18, wherein the switching regulator comprises a first switch and a second switch driving a switch

output node, the first switch being turned on to decrease the current provided to the switch output node and the second switch being turned on to increase the current provided to the switch output node, the first switch being controlled by a first switch control signal and the second switch being controlled by a second switch control signal, and the switching regulator further comprises an error amplifier in the feedback control loop, the error amplifier coupled to compare a voltage indicative of the output voltage to a reference voltage and generate an error output voltage.

20. The method of Claim 19, wherein the switching regulator comprises a voltage mode buck regulator and the loop gain is given as $V_{Ref}A_{VEA}V_{IN}/V_{OUT}$, where V_{Ref} is the reference voltage, A_{VEA} is the gain of the error amplifier, V_{IN} is the input voltage, and V_{OUT} is the output voltage, and wherein the second function is given as $(1 + t_{ON,M2}/t_{ON,M1})$ which is equivalent to V_{OUT}/V_{IN}, where $t_{ON,M2}$ represents the on-time of the second switch and $t_{ON,M1}$ represents the on-time of the first switch.

21. The method of Claim 20, wherein the switching regulator is being operated in a continuous conduction mode and the second function is given as $(t_{ON,M2}/T_{cycle})$ which is equivalent to V_{OUT}/V_{IN}, wherein T_{cycle} is the system clock cycle time of the switching regulator.